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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,851	06/24/2003	Tetsuya Makino	1100.68107	9306

7590 12/13/2005

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EXAMINER	
GOOD JOHNSON, MOTILEWA	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,851	MAKINO ET AL.	
	Examiner	Art Unit	
	Motilewa Good-Johnson	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19 and 20* is/are rejected.

7)☒ Claim(s) *18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the scanning circuit and polarities having a complementary relationship must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 17 and 19, 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Konno et al., U.W. Patent Number 6.940,481 B2.

Regarding claims 1 and 7, Konno discloses a driving method and apparatus for a liquid crystal display apparatus, including a substrate on which pixel electrodes (210) and switching elements for on/of controlling voltage application to said pixel electrodes are arranged in matrix form (col. 2, line 58 – col. 3, line 9); a substrate on which a counter electrode is provided (col. 5, lines 55-56); and a liquid crystal material having a spontaneous polarization sealed in a gap between said substrates (col. 5, line 52), by applying a data voltage (col. 8, lines 55-64) across said pixel electrodes and said counter electrode during an ON period of said switching elements(203, col. 8, lines 18-20) and holding the data voltage during an OFF period so as to control a light transmission rate of said liquid crystal material which is determined by the data voltage, wherein said driving method applies a reset voltage of a constant value in a first half

period of said ON period, and applies said data voltage in a second half period of said 0N period (col. 10, lines 11-20)

Regarding claim 2, Konno discloses wherein said first half period is substantially 1/2 of said ON period (col. 6, lines 4-6)

Regarding claim 3, Konno discloses wherein said switching elements are on/off controlled at predetermined time intervals, data voltages of opposite polarities are applied alternately in preceding and following ON periods, and a reset voltage with a polarity opposite to the data voltage is applied in the same ON period (col. 9, lines 39-54)

Regarding claim 4, Konno discloses wherein said reset voltage is 0 V (col. 16, line 31)

Regarding claim 5, Konno discloses wherein said first half period is substantially 1/2 of said 0N period (col. 6, lines 4-6)

Regarding claim 6, Konno discloses wherein said reset voltage is 0 V (col. 15, line 31)

Regarding claim 8, Konno discloses wherein said switching elements are on/off controlled at predetermined time intervals, said data voltage applied in an ON period has a polarity opposites to data voltages applied in ON periods preceding and following said ON period, and said reset voltage has a polarity opposite to the data voltage in the same ON period (col. 9, lines 39-54)

Regarding claim 9, Konno discloses wherein said first half period is substantially 1/2 of said ON period (col. 6, lines 4-6)

Regarding claim 10, Konno discloses further comprising: a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and a scanning circuit having a plurality of output portions for on/off controlling said switching elements; wherein said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit (col. 12, line 65 - col. 13, line 10, figure 9)

Regarding claim 11, Konno discloses further comprising a control circuit for controlling scanning of said scanning circuit, wherein said scanning circuit comprises: means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and means for generating a scanning start signal, having a signal

width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period (figure 1)

Regarding claim 12, Konno discloses wherein said first half period is substantially 1/2 of said ON period (col. 6, lines 4-6)

Regarding claim 13, Konno discloses further comprising: a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and a scanning circuit having a plurality of output portions for on/of controlling said switching elements; wherein said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit (col. 12, line 65 – col. 13, line 10, figure 9)

Regarding claim 14, Konno discloses further comprising a control circuit for controlling scanning of said scanning circuit, wherein said scanning circuit comprises: means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and means for generating a scanning start signal, having a signal width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period (figure 1)

Regarding claim 15, Konno discloses wherein said reset voltage is 0 V (col. 16, line 31)

Regarding claim 16, further comprising: a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns among pixels in a matrix row, and a second scanning line connected with the switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and a scanning circuit having a plurality of output portions for on/off controlling said switching elements; wherein said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit (col. 12, line 65 – col. 13, line 10, figure 9)

Regarding claim 17, further comprising a control circuit (105) for controlling scanning of said scanning circuit, wherein said scanning circuit comprises: means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and means for generating a scanning start signal, having a signal width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period.

Regarding claim 19, Konno discloses further comprising: a first scanning line connected with the switching elements connected to pixels in odd-numbered matrix columns among pixels in a matrix row, and a second scanning line connected with the

switching elements connected to pixels in even-numbered matrix columns in the same matrix row; and a scanning circuit having a plurality of output portions for on/off controlling said switching elements; wherein said first scanning line and said second scanning line are alternately connected to the output portions of said scanning circuit (col. 12, line 65 – col. 13, line 10, figure 9)

Regarding claim 20, Konno discloses further comprising a control circuit for controlling scanning of said scanning circuit, wherein said scanning circuit comprises: means for generating an operation clock signal for determining a scanning frequency of said scanning circuit; and means for generating a scanning start signal, having a signal width equal to a two-clock period of said operation clock signal, for determining scanning start timing of said scanning circuit and said ON period (figure 1)

Allowable Subject Matter

4. Claim 18 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to render obvious scanning frequencies of first scanning circuit and second scanning circuit so that polarities have a complementary relationship.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Motilewa Good-Johnson whose telephone number is (571) 272-7658. The examiner can normally be reached on Monday, Tuesday and Wednesday 9:00 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Motilewa Good-Johnson
Examiner
Art Unit 2677

mgj

AMR A. AWAD
PRIMARY EXAMINER